ENGR 262 Digital Logic Design
Homework 3

Due at 4:00 PM on Friday, February 24th.

Show all your work for each problem.

Simplifying Boolean Function Using K-Map

1. For the K-map shown below, write the simplified expression, and draw the simplest possible circuit

wx \ yz	00	01	11	10
00		1	1	
01	1			1
11	1			1
10		1	1	

2. For the K-map shown below, write the simplified expression, and draw the simplest possible circuit

wx \ yz	00	01	11	10
00	1	1	1	1
01	1	1	1	
11	1	1		
10	1			

3. For the given Boolean functions, write the simplified functions using K-Map,
   a. $F(A,B,C,D) = AC'D' + A'C + ABC + AB'C + A'C'D'$
   b. $F(A,B,C,D) = A'B'C'D + CD + AC'D$

4. Minimize the given functions with its don't care:
   a. $f(w,x,y,z) = \Sigma m(1,3,11,15) + \Sigma d(5,7,10,12,14)$.
   b. $f(x_1,x_2,x_3) = \sum m(1,4,7) + \sum d(2,5)$
   c. $f(x_1,x_2,x_3,x_4) = \sum m(0,2,8,9,10,15) + \sum d(1,3,6,7)$
   d. $f(x_1,x_2,x_3,x_4) = \sum m(0,2,4,6,7,9) + \sum d(10,11)$
   e. $g(x_1,x_2,x_3,x_4) = \sum m(2,4,9,10,15) + \sum d(0,13,14)$

Design of Combinational Circuits

The word "**Design**" includes

- Truth table, K-map of each output bit, and logic diagram of the simplified output functions. For simplicity and clarity, draw a separate logic diagram for each output bit. You may also use logic gates with any number of inputs.
- Writing the **behavioral** Verilog-HDL design.

5. Design a combinational circuit with three inputs x, y, and z, and three outputs A, B, and C. When the binary inputs is 0, 1, 2, or 3, the binary output is two greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is three less than the input.

6. Design a 3-bit majority circuit. A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise.

7. Design a 4-bit combinational circuit 2's complementer (the circuit generates the 2's complement of the 4-bit input).

Design of a 2-bit Calculator using Verilog-HDL

8. Design a 2-bit calculator using modular design of multiple behavioral modules. The calculator has two inputs *x* and *y*; each is of 2-bit. The calculator has a 4-bit output *z*. The calculator has another 2-bit input *select*. The functions of the calculator is described by the table below;

Select	***z***
0	$x+y$
1	$x-y$
2	$x*y$

a. Write the behavioral Verilog-HDL of the adder (define the output as 4-bit)

b. Write the behavioral Verilog-HDL of the subtractor (define the output as 4-bit)

c. Write the behavioral Verilog-HDL of the multiplier (define the output as 4-bit)

d. Write the behavioral Verilog-HDL of 4-bit, 2x1 multiplexer

e. Draw the block diagram of connecting the different blocks of the calculator

f. Combine (instantiate) the previous modules to form the 2-bit calculator